CLAIMS

1. A semiconductor integrated circuit device having integrated circuits with different functions integrated into one semiconductor chip, the semiconductor integrated circuit device comprising:

a semiconductor chip;

a separating region, formed in the semiconductor chip, for separating the semiconductor chip into a plurality of integrated circuit formation regions, said separating region being exposed to entire side faces of the semiconductor chip; and

integrated circuits formed in the integrated circuit formation regions, respectively, said integrated circuits having different functions, at least one of the integrated circuits performing a function fluctuating a potential of the integrated circuit formation region in which said at least one of the integrated circuits is formed.

2. The semiconductor integrated circuit device according to claim 1, wherein said integrated circuits include at least two of a non-volatile memory circuit, an analog circuit, a digital circuit, a digital/analog conversion circuit, a static memory circuit and a dynamic memory circuit, and said at least one of the integrated circuits which performs the function fluctuating the potential of the integrated circuit formation region includes at least one of

a non-volatile memory circuit and an analog circuit.

3. The semiconductor integrated circuit device according to claim 2, wherein said separating region is formed of a semiconductor substrate of a first conductivity type, and each of the integrated circuit formation regions is a first well of a second conductivity type formed in the substrate.

4. The semiconductor integrated circuit device according to claim 3, wherein a second well of the first conductivity type, which is supplied with a negative potential, is formed in said first well, and at least one of an input/output circuit and an interface circuit is formed in the second well.

5. A semiconductor integrated circuit device having integrated circuits with different functions integrated into one semiconductor chip, the semiconductor integrated circuit device comprising:

a semiconductor chip;

a separating region, formed in the semiconductor chip, for separating the semiconductor chip into a plurality of integrated circuit formation regions, said separating region being exposed to entire side faces of the semiconductor chip; and

integrated circuits formed in the integrated circuit formation regions, respectively, said integrated circuits having dedicated power supplies.

6. The semiconductor integrated circuit device

according to claim 5, wherein said integrated circuits include at least two of a non-volatile memory circuit, an analog circuit, a digital circuit, a digital/analog conversion circuit, a static memory circuit and a dynamic memory circuit.

7. The semiconductor integrated circuit device according to claim 6, wherein said separating region is formed of a semiconductor substrate of a first conductivity type, and each of the integrated circuit formation regions is a first well of a second conductivity type formed in the substrate.

8. The semiconductor integrated circuit device according to claim 7, wherein a second well of the first conductivity type, which is supplied with a negative potential, is formed in said first well, and at least one of an input/output circuit and an interface circuit is formed in the second well.

9. A method of testing a semiconductor integrated circuit device comprising a semiconductor chip; a separating region, formed in the semiconductor chip, for separating the semiconductor chip into a plurality of integrated circuit formation regions, said separating region being exposed to entire peripheral side faces of the semiconductor chip; and integrated circuits formed in the integrated circuit formation regions, respectively, said integrated circuits having dedicated power supplies,

wherein while at least one of the integrated circuits is being tested, power is supplied to only the integrated circuit being tested, and no power is supplied to the other integrated circuits.

10. The method of testing the semiconductor integrated circuit device, according to claim 9, wherein said integrated circuit includes at least one of a non-volatile memory circuit and a dynamic memory circuit, and at least one of an analog circuit, a digital circuit and a digital/analog conversion circuit, and

while a test is being conducted to specify a defective row and a defective column in said at least one of the non-volatile memory circuit and the dynamic memory circuit, no power is supplied to the other integrated circuits.

11. A semiconductor integrated circuit comprising device:

a semiconductor substrate of a first conductivity type;

at least one first well of a second conductivity type, formed in the semiconductor substrate;

an integrated circuit formed in the first well;

a power supply system including a high-potential power line and a low-potential power line for supplying an operational voltage to the integrated circuit;

a bias system for supplying a bias potential to

the semiconductor substrate, the bias system including a bias line separated from the high-potential power line and the low-potential power line;

a first pad connected to the bias line;

a second pad connected to the high-potential power line; and

a third pad connected to the low-potential power line.

12. The semiconductor integrated circuit device according to claim 11, wherein when the integrated circuit is tested, the operational voltage and the bias potential are supplied independently.

13. The semiconductor integrated circuit device according to claim 12, wherein in the state in which a plurality of semiconductor chips each composed of the integrated circuit are formed on a semiconductor wafer, the integrated circuits of the semiconductor chips are tested at the same time.

14. The semiconductor integrated circuit device according to claim 11, further comprising an external lead connected to the first pad and one of the second and third pads.

15. The semiconductor integrated circuit device according to claim 11, wherein a second well of the first conductivity type is formed in the first well, and a bias potential supplied to the second well is equal to a bias potential supplied to the semiconductor

substrate.

16. The semiconductor integrated circuit device according to claim 11, wherein said semiconductor substrate constitutes a semiconductor wafer.

17. The semiconductor integrated circuit device according to claim 11, wherein there are provided at least two of said first wells, at least two of said integrated circuits with different functions are formed in at least two of said first wells, and a semiconductor device system constituted by connecting the integrated circuits with the different functions is integrated in the semiconductor substrate.

18. The semiconductor integrated circuit device according to claim 17, wherein said integrated circuits with the different functions are selected from a group consisting of a processor, a dynamic RAM, a static RAM, an EEPROM, a D/A converter, an analog circuit and a logic circuit.

19. A tester for a semiconductor integrated circuit, the tester comprising:

a supply voltage generator, associated with a plurality of semiconductor integrated circuit device chips to be tested at a time, for generating a supply voltage for operating integrated circuits on each semiconductor integrated circuit device chip;

a detector for detecting a variation in supply voltage for each semiconductor integrated circuit

device chip, while the semiconductor integrated circuit device chips are being tested;

a judgement circuit device for determining whether the variation in supply voltage detected for each chip falls within a predetermined range of allowance; and

a switch control circuit and driver circuit for shutting off, when it has been determined that the variation in supply voltage detected for each chip falls outside the predetermined range of allowance, the supply of the supply voltage to the chip with the variation in supply voltage outside the predetermined range of allowance.

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